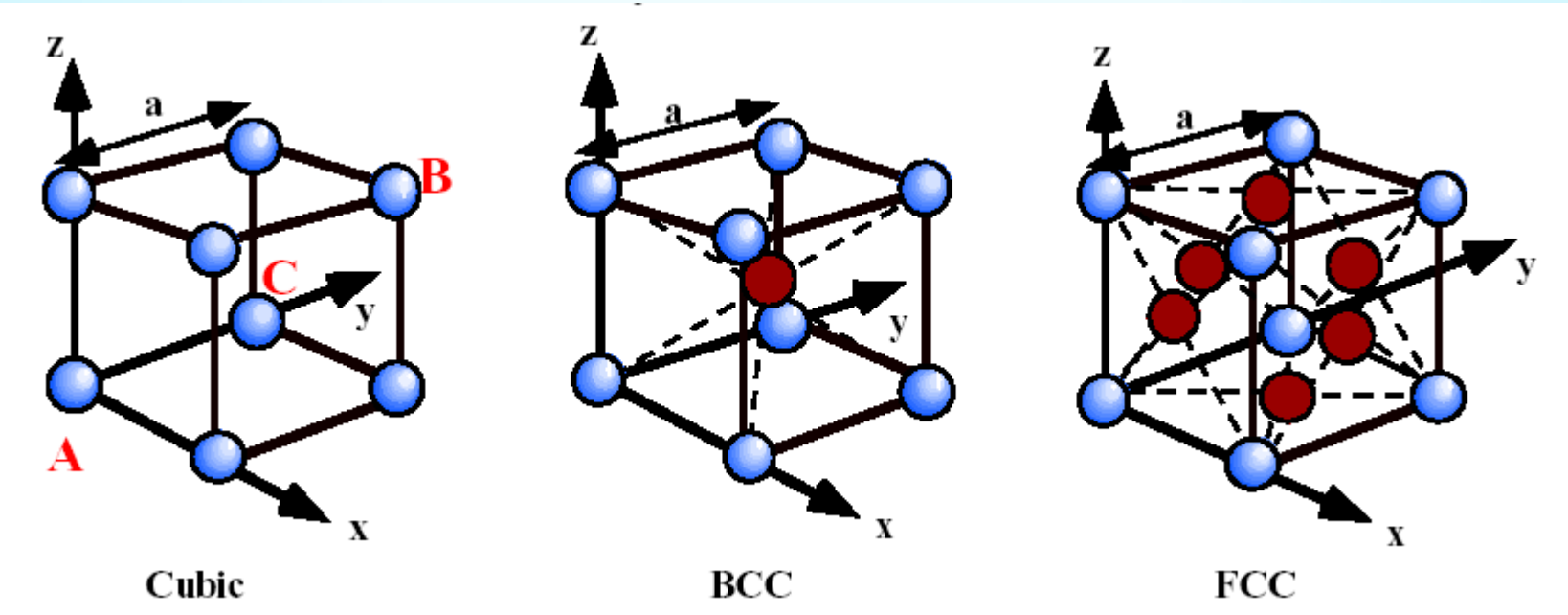
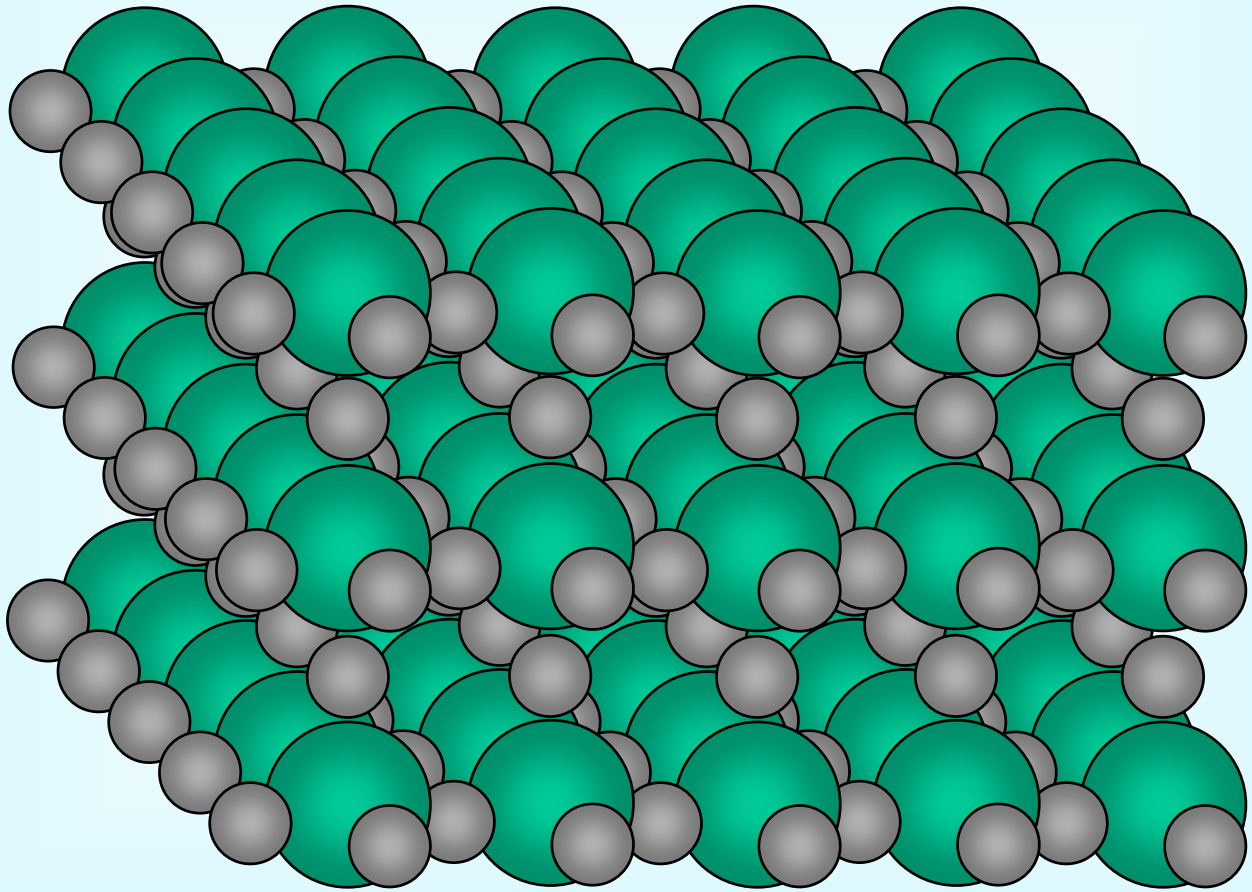
Crystal Structure and Growth

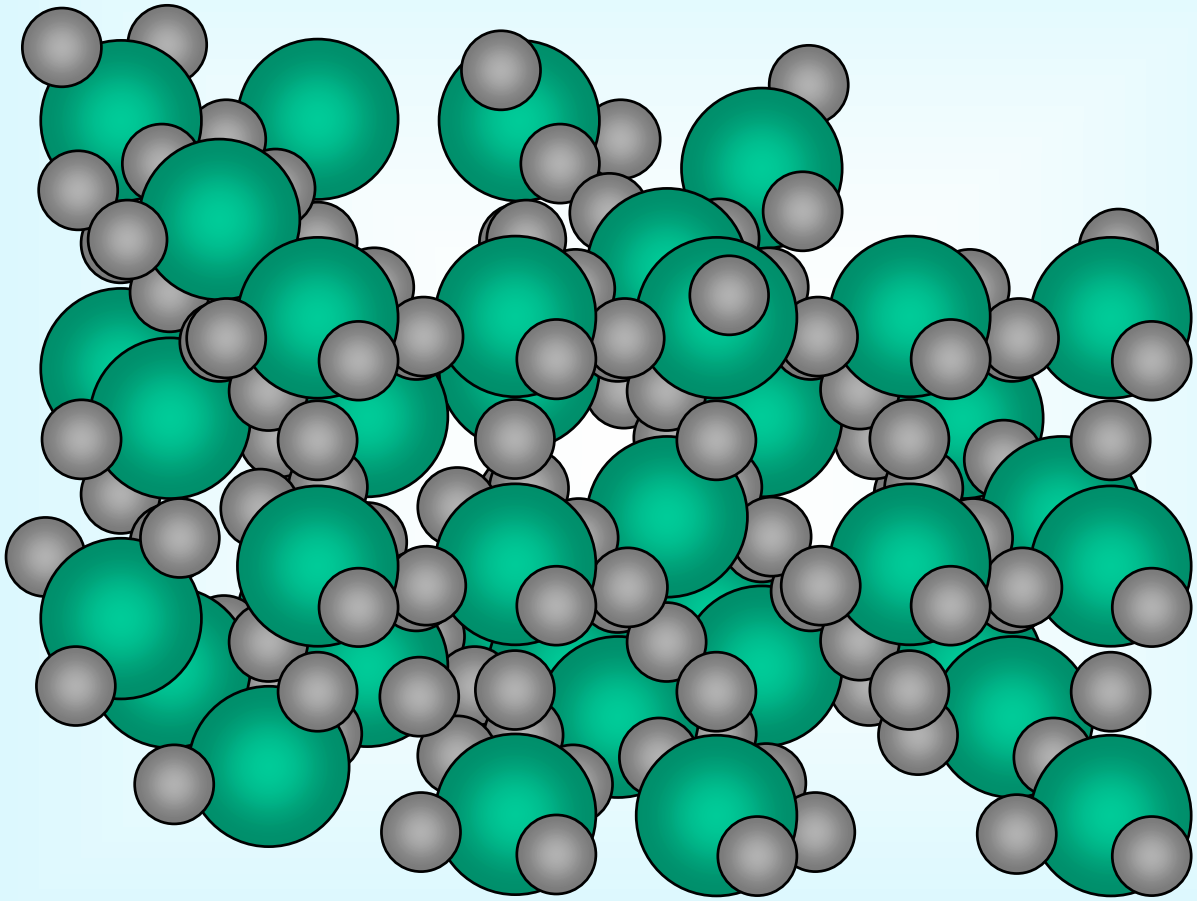


Source: USNA EE 452 Course on IC Technology

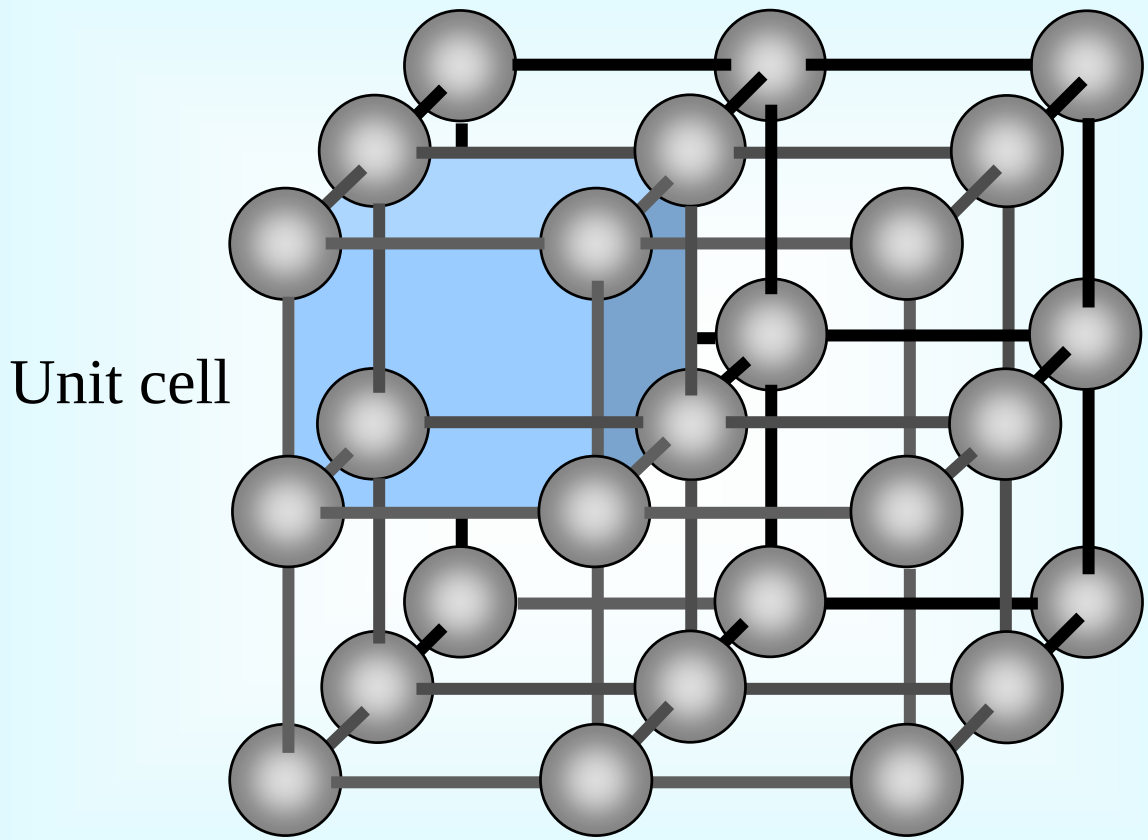
Atomic Order of a Crystal Structure



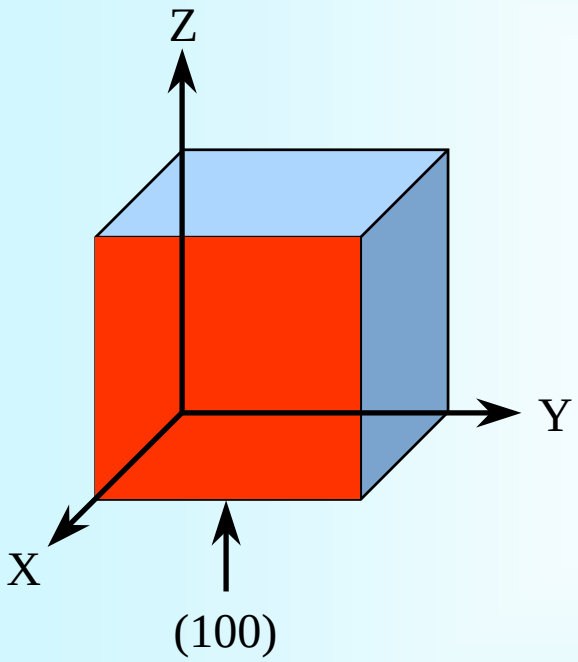
Amorphous Atomic Structure

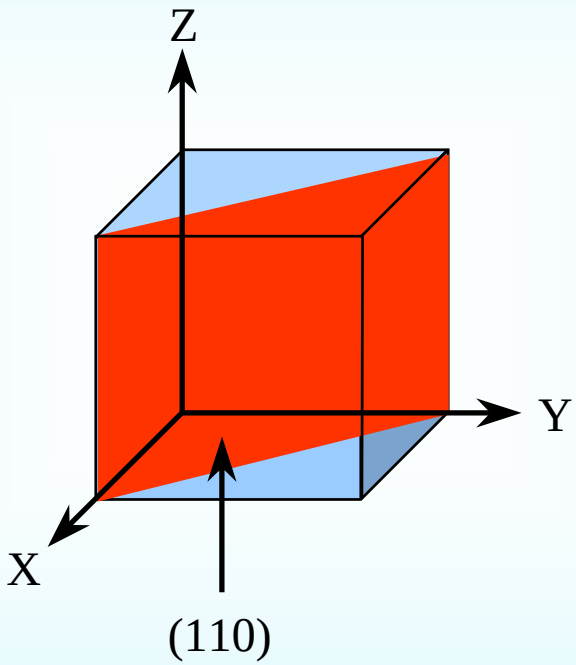


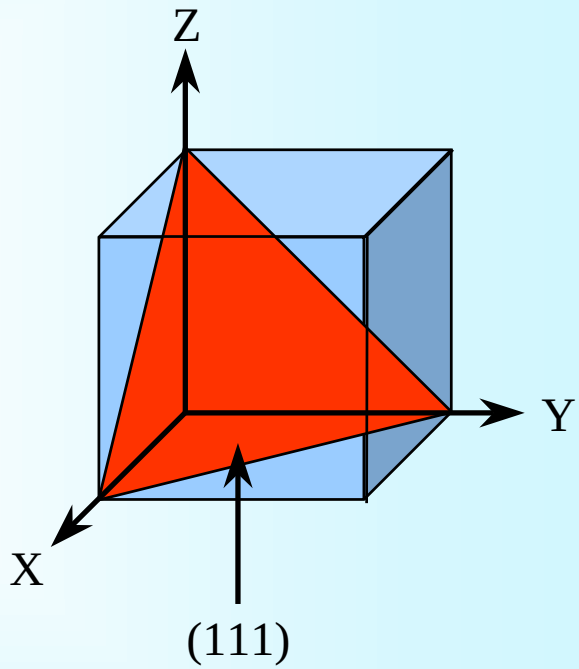
Unit Cell in 3-D Structure



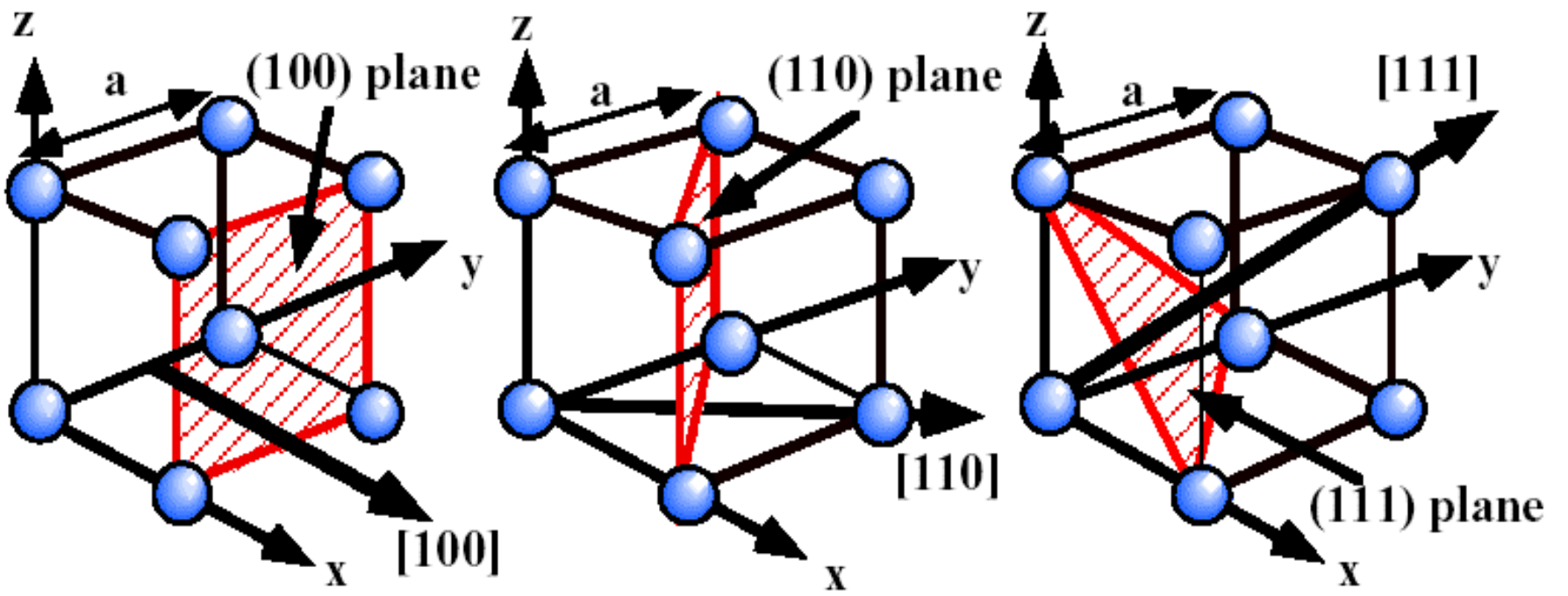
Miller Indices of Crystal Planes







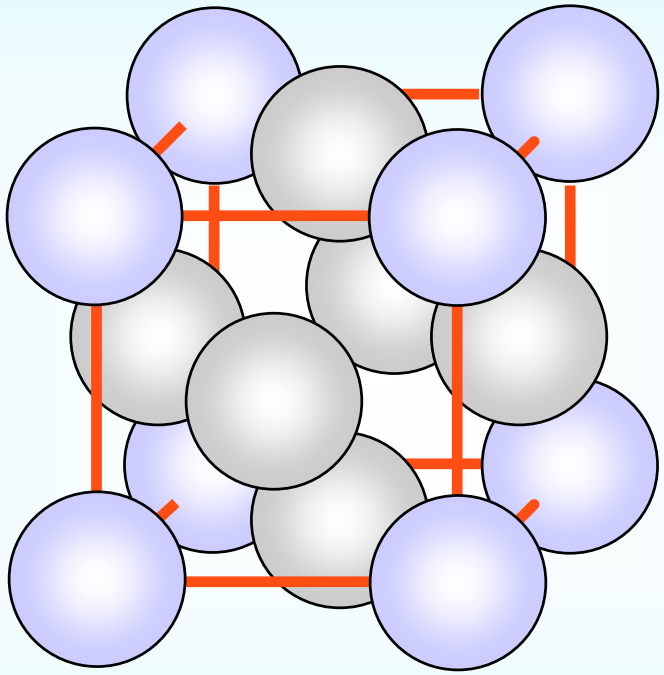
Crystal Planes



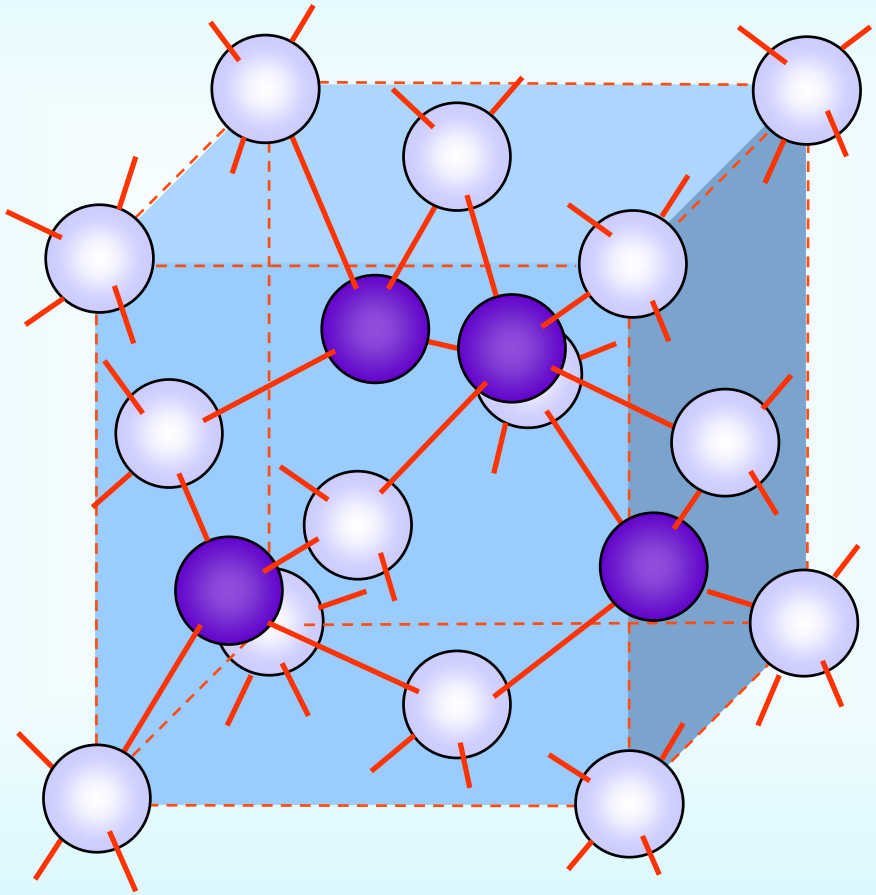
Crystals are characterized by a unit cell which repeats in the x, y, z directions.

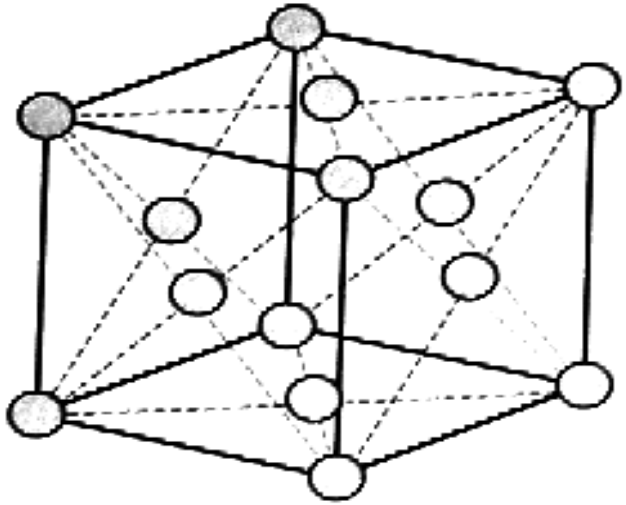
- **Planes and directions are defined using x, y, z coordinates.**
- **[111] direction is defined by a vector of 1 unit in x, y and z.**
- **Planes defined by "Miller indices" – their normal direction.**

Faced-centered Cubic (FCC) Unit Cell

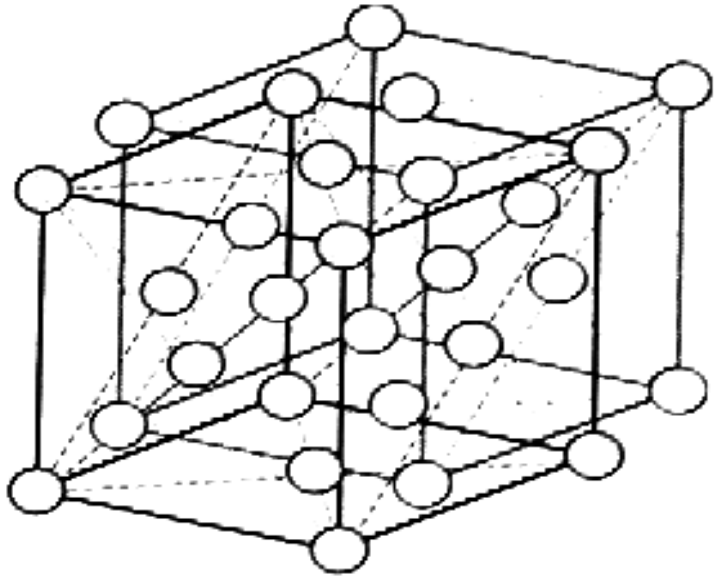


Silicon Unit Cell: FCC Diamond Structure

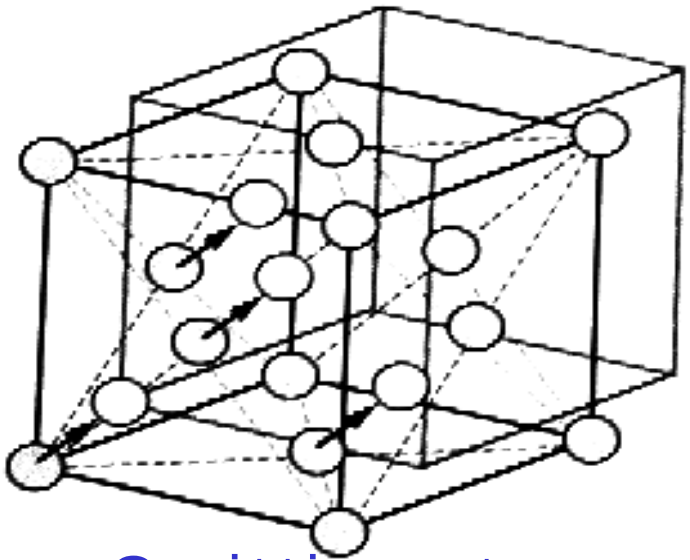




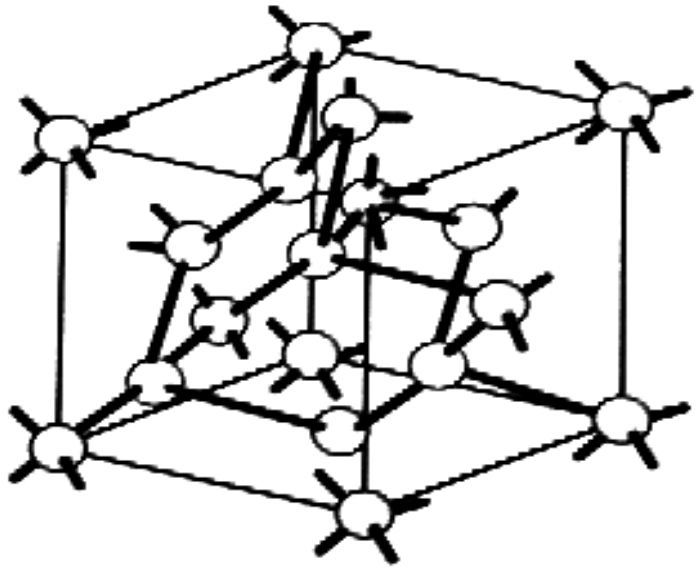
Basic FCC Cell



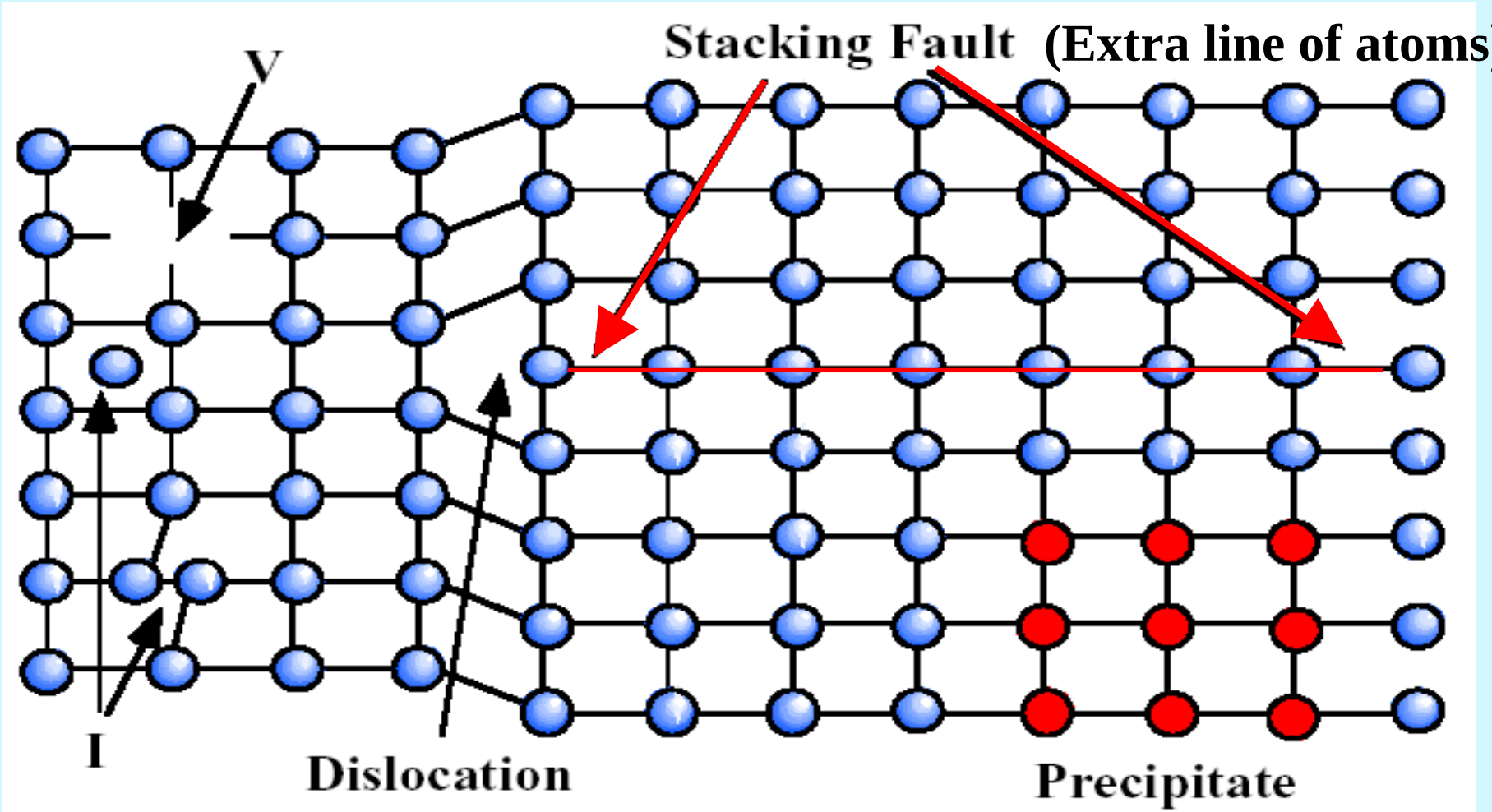
Merged FCC Cells



Omitting atoms outside Cell



Bonding of Atoms



Various types of defects can exist in a crystal (or can be created by processing steps). In general, these cause electrical leakage and are result in poorer devices.

Bulk Silicon Processing

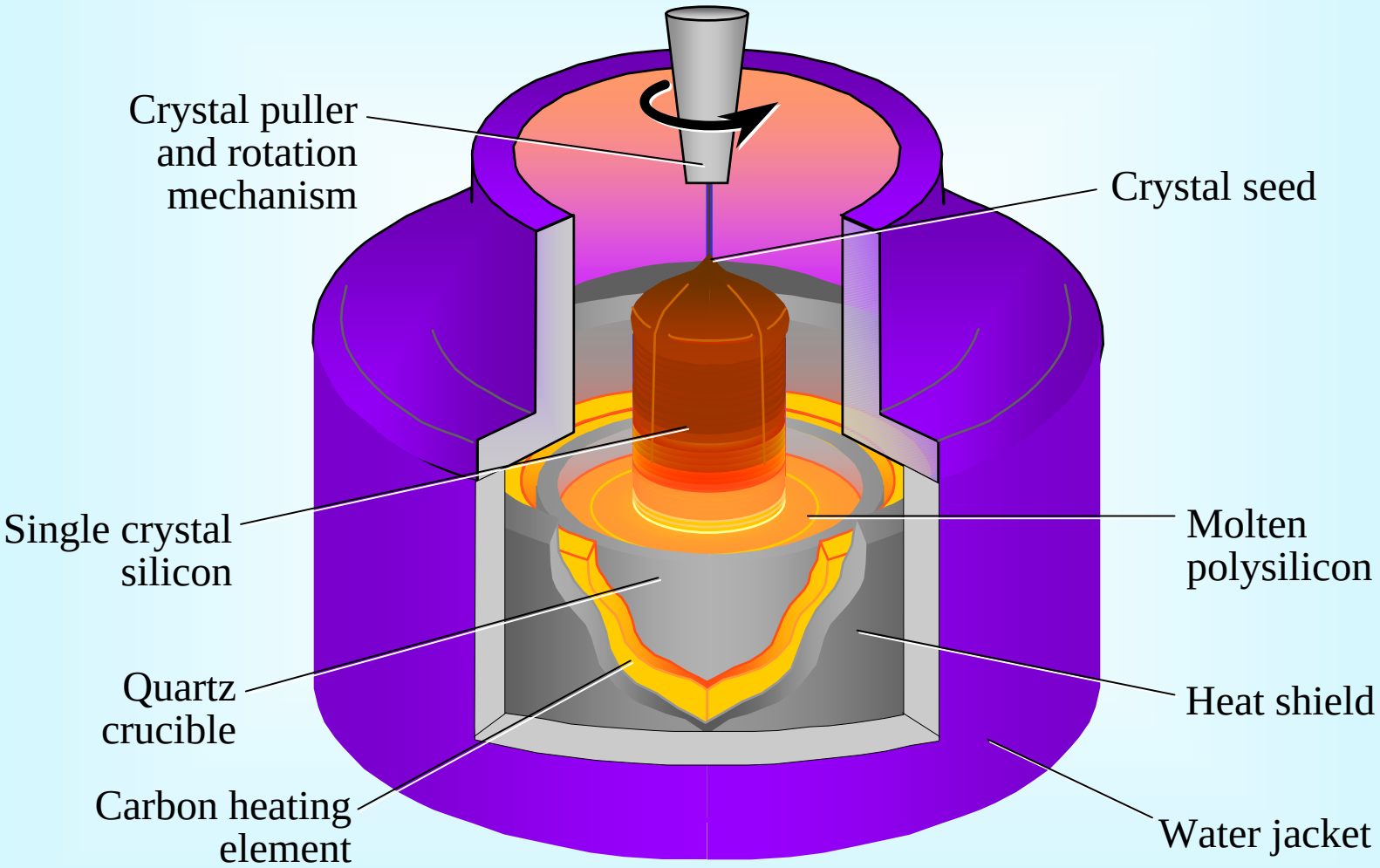
- **Si is purified from SiO_2 (sand) by refining, distillation and CVD.**
- **Bulk silicon is first processed in poly-crystalline form**
- **Crystal growth process used to obtain single-crystal form**
- **It contains < 1 ppb impurities. Pulled crystals contain O (~10^{18} cm^{-3}) and C (~10^{16} cm^{-3}), plus dopants placed in the melt.**

Silicon Processing

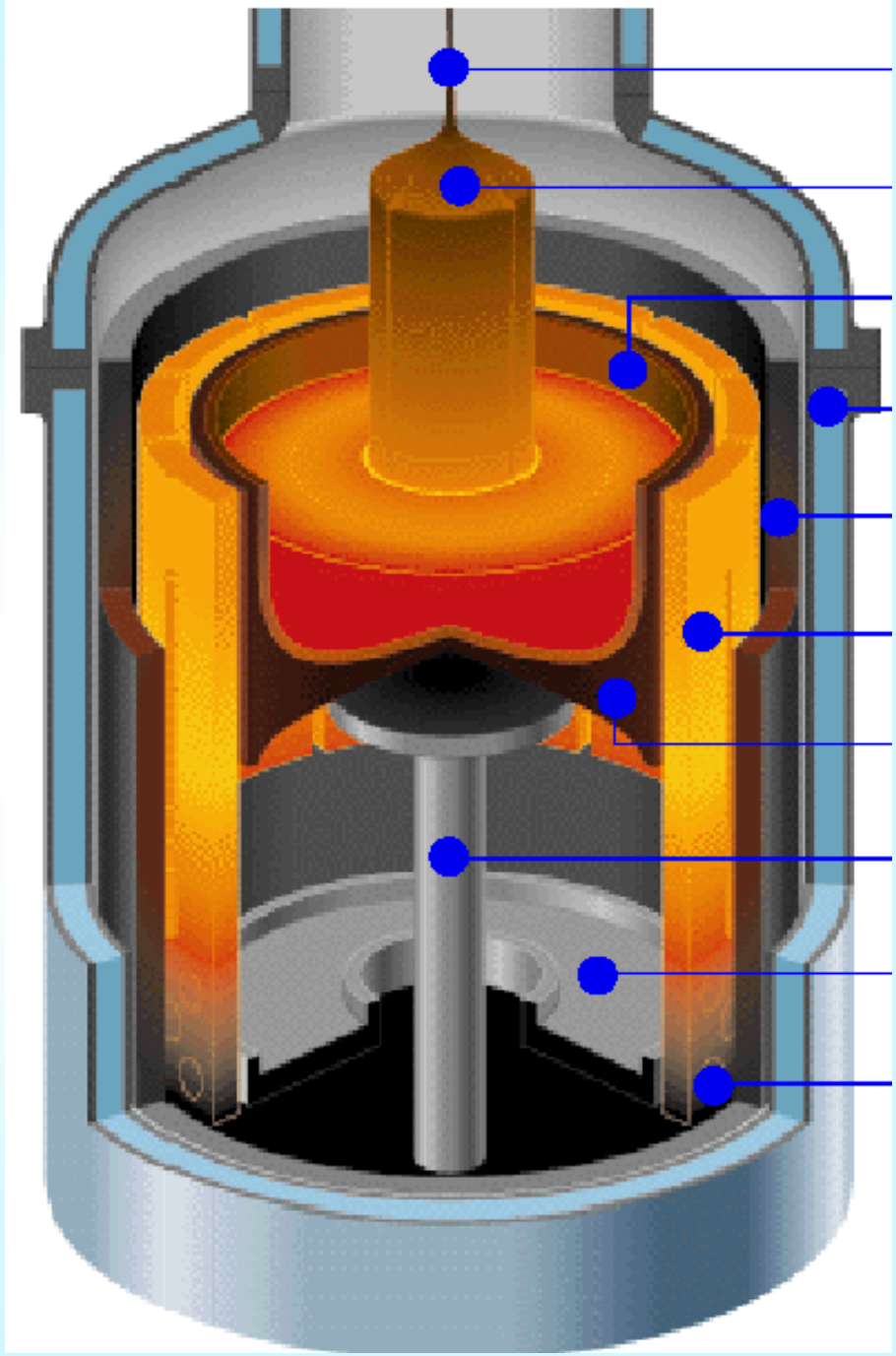
First produce highly pure, poly-crystalline form

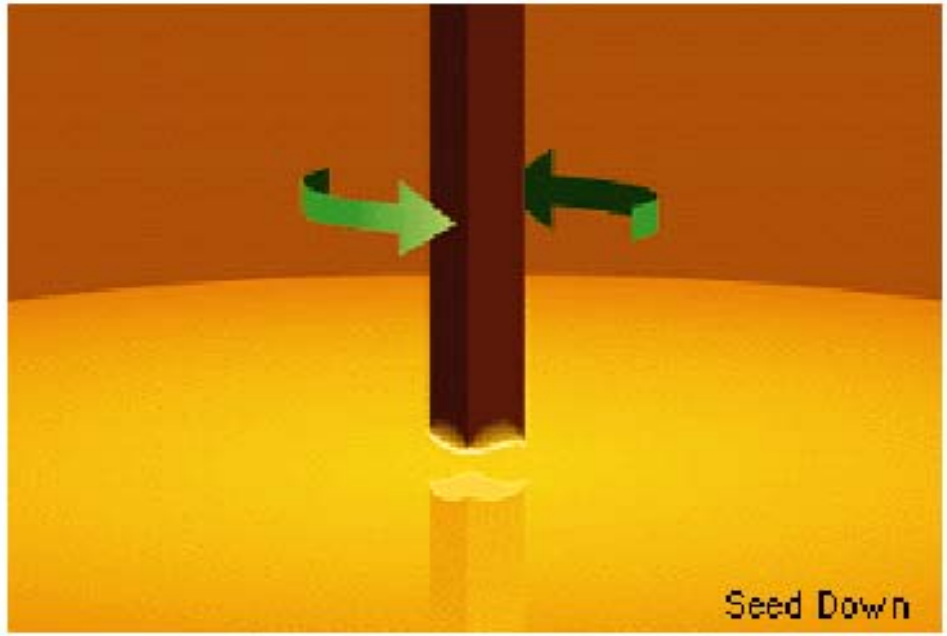
Steps to Obtaining Semiconductor Grade Silicon (SGS)		
Step	**Description of Process**	**Reaction**
1	Produce metallurgical grade silicon (MGS) by heating silica with carbon (furnace)	$SiC\ (s) + SiO_2\ (s) \rightarrow Si\ (l) + SiO(g) + CO\ (g)$
2	Purify MG silicon through a chemical reaction to produce a silicon-bearing gas of trichlorosilane ($SiHCl_3$)	$Si\ (s) + 3HCl\ (g) \rightarrow SiHCl_3\ (g) + H_2\ (g) + heat$
3	$SiHCl_3$ and hydrogen react in a CVD process to obtain pure semiconductor- grade silicon (SGS)	$2SiHCl_3\ (g) + 2H_2\ (g) \rightarrow 2Si\ (s) + 6HCl\ (g)$

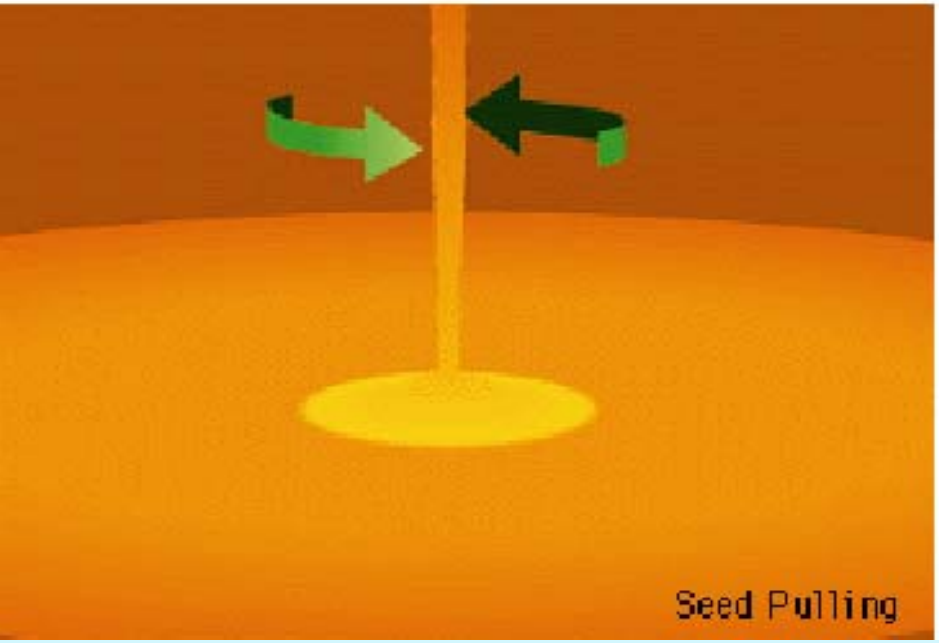
Single Crystal Processing: Czochralski Crystal Puller

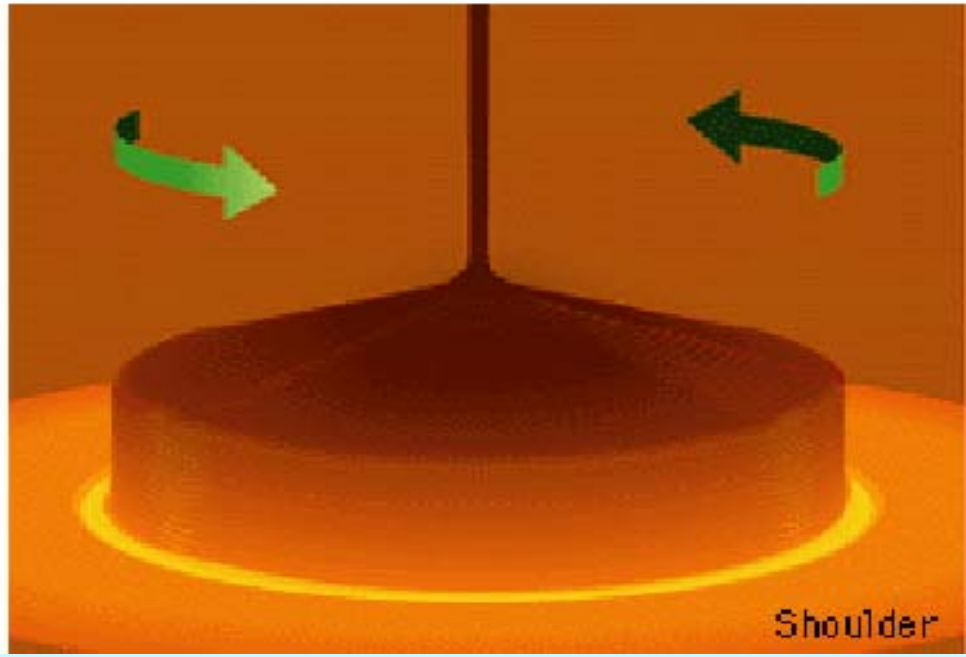


- All Si wafers come from “Czochralski” grown crystals.
- Polysilicon is melted, then held just below 1417 °C, and a single crystal seed starts the growth.
- Pull rate, melt temperature and rotation rate control the growth

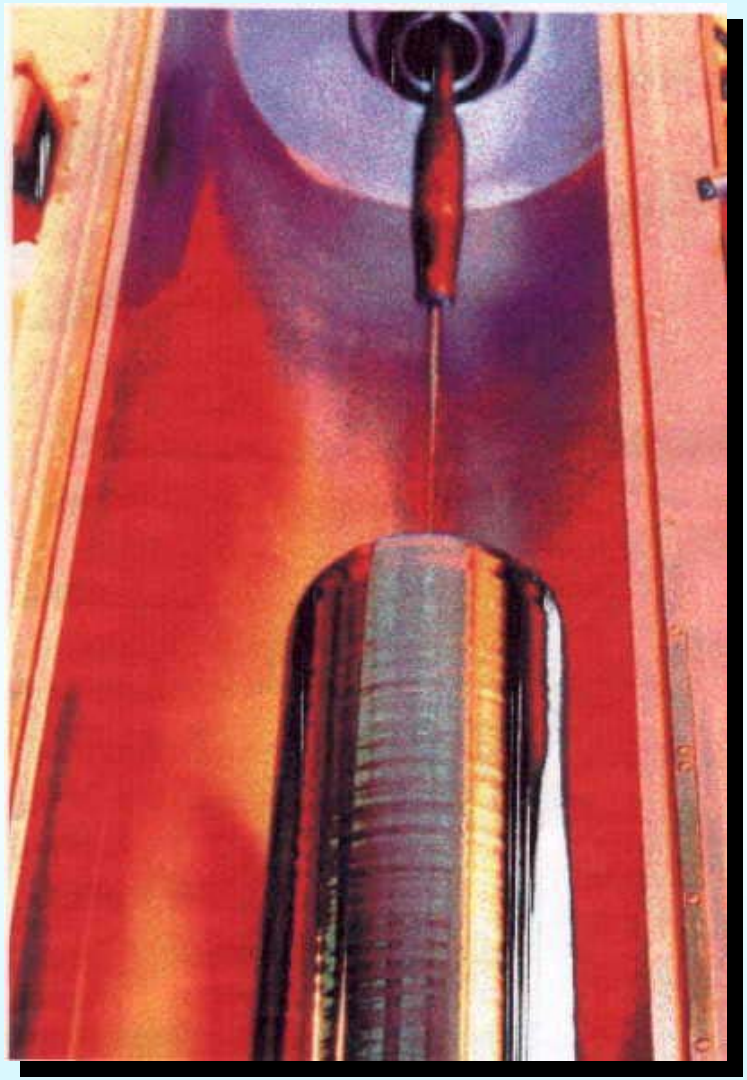



Seed Down


Seed Pulling

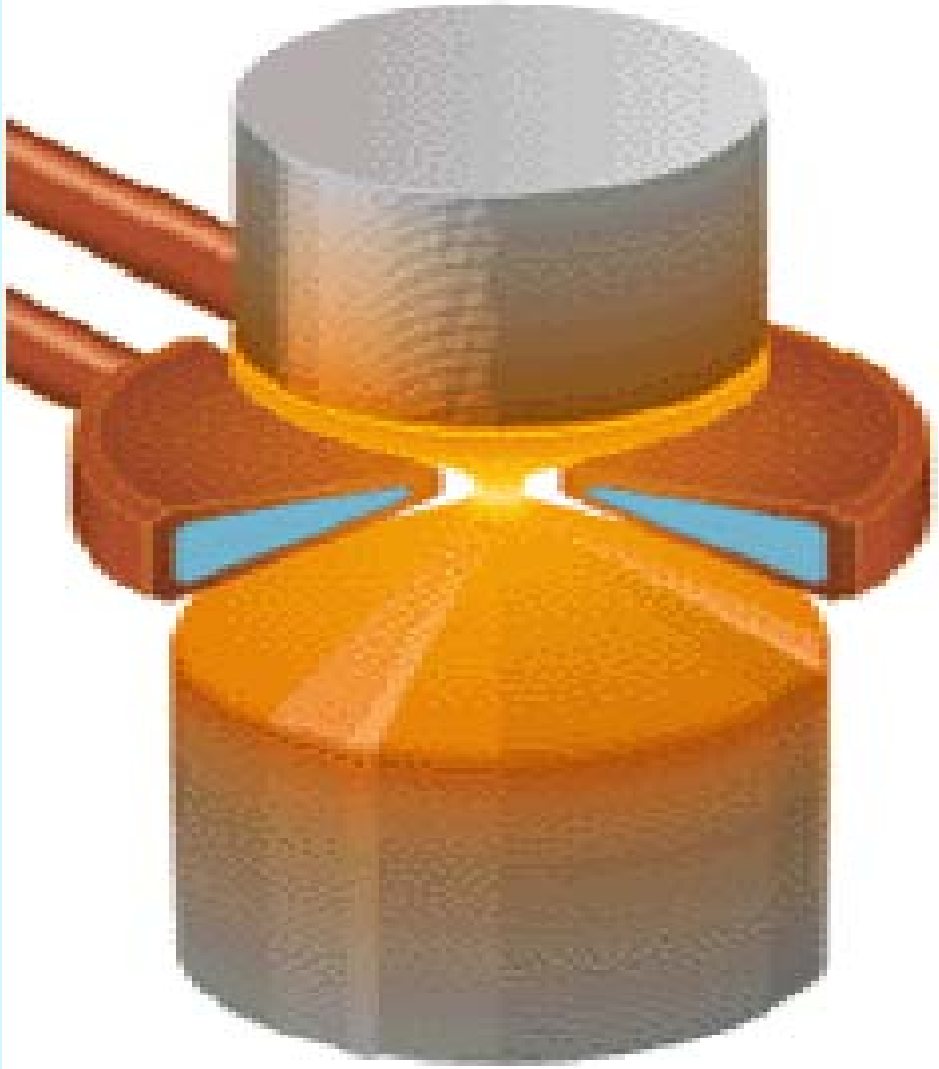

Shoulder

Silicon Ingot Grown by CZ Method



Photograph courtesy of Kayex Corp., 300 mm Si ingot

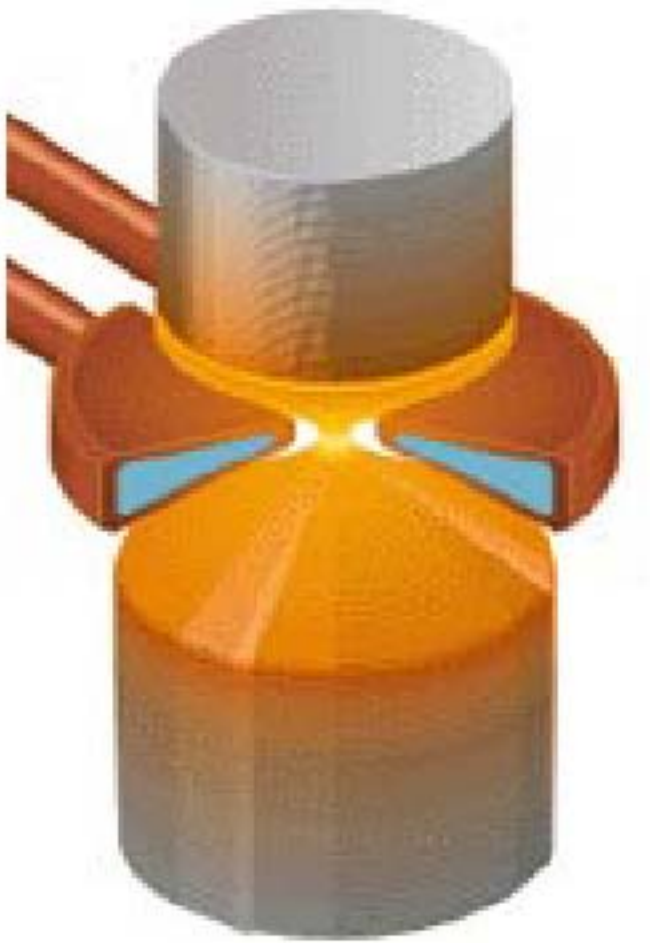
An alternative process is the "Float Zone" process which can be used for refining or single crystal growth.

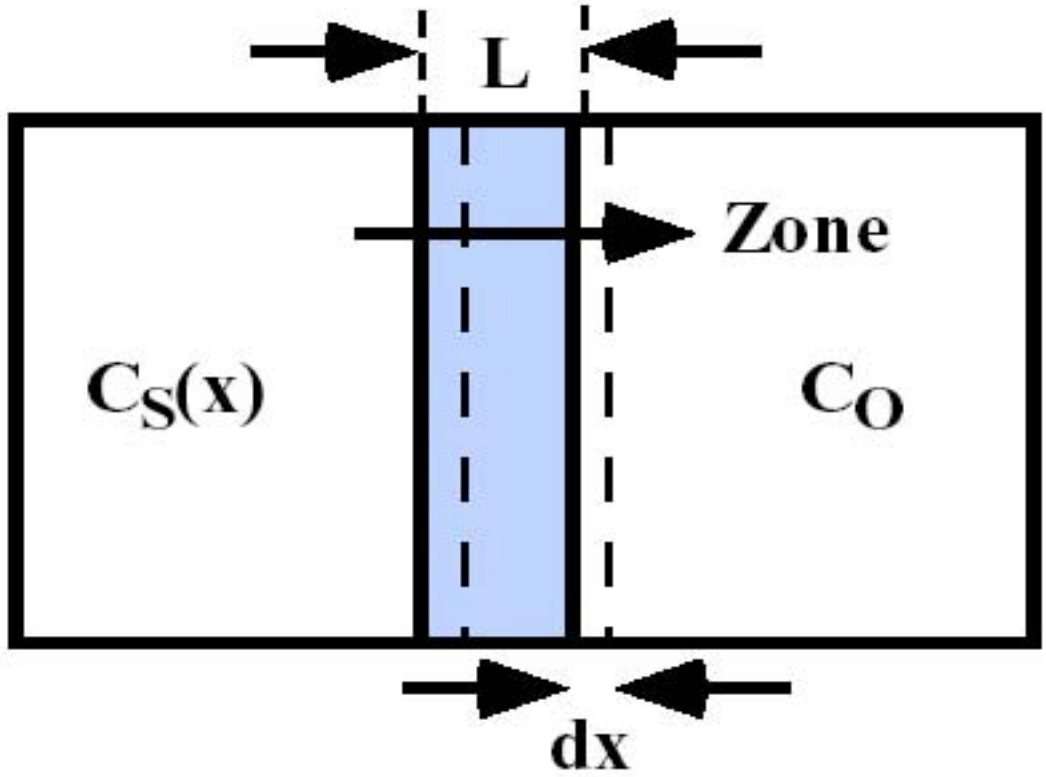


Polysilicon Ingot

RF Coil

Single Crystal Si





• In the float zone process, dopants and other impurities are rejected by the regrowing silicon crystal. Impurities tend to stay in the liquid and refining can be accomplished, especially with multiple passes.

Float Zone Crystal Growth

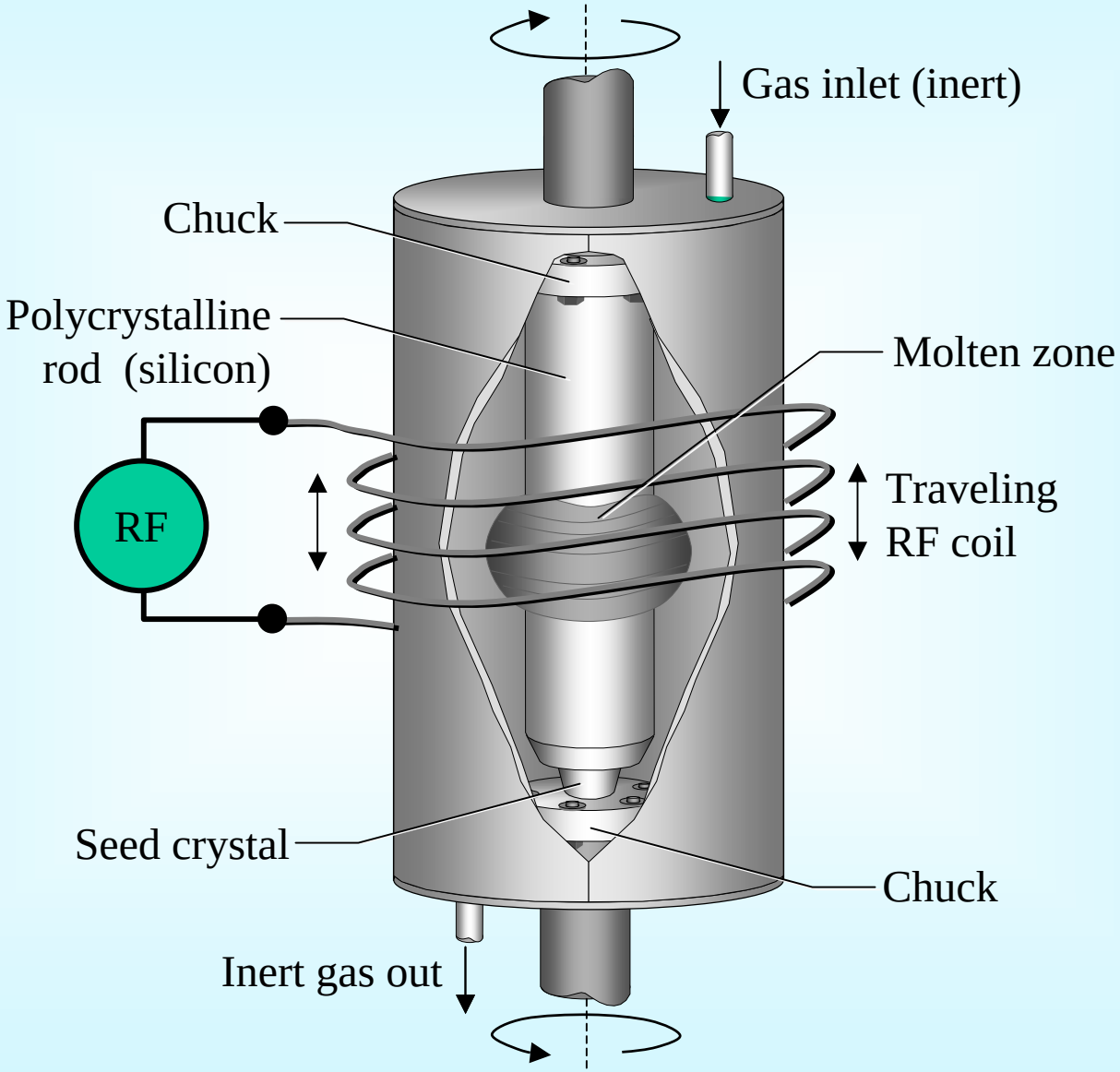


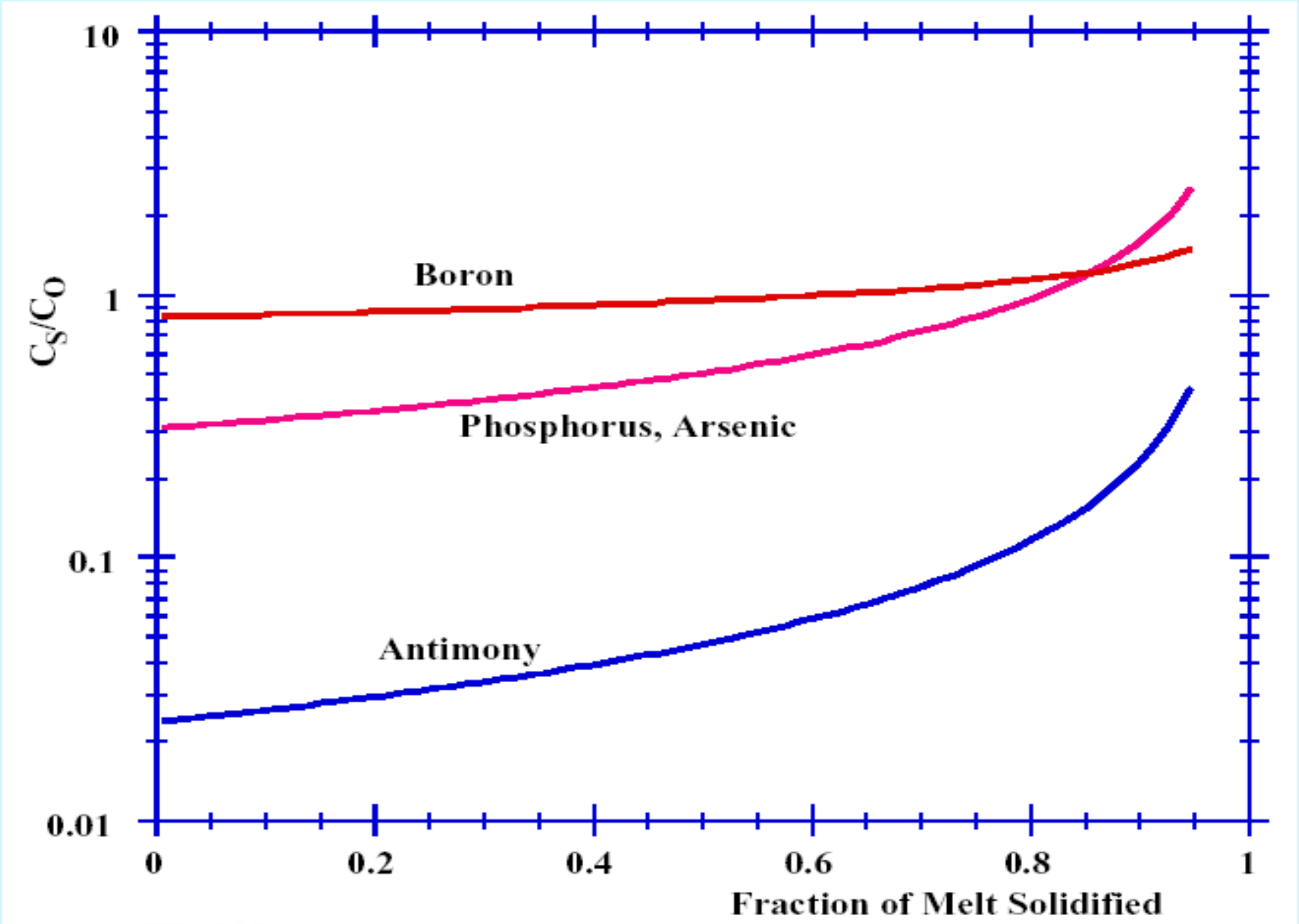
Figure 4.11

Dopant Concentration

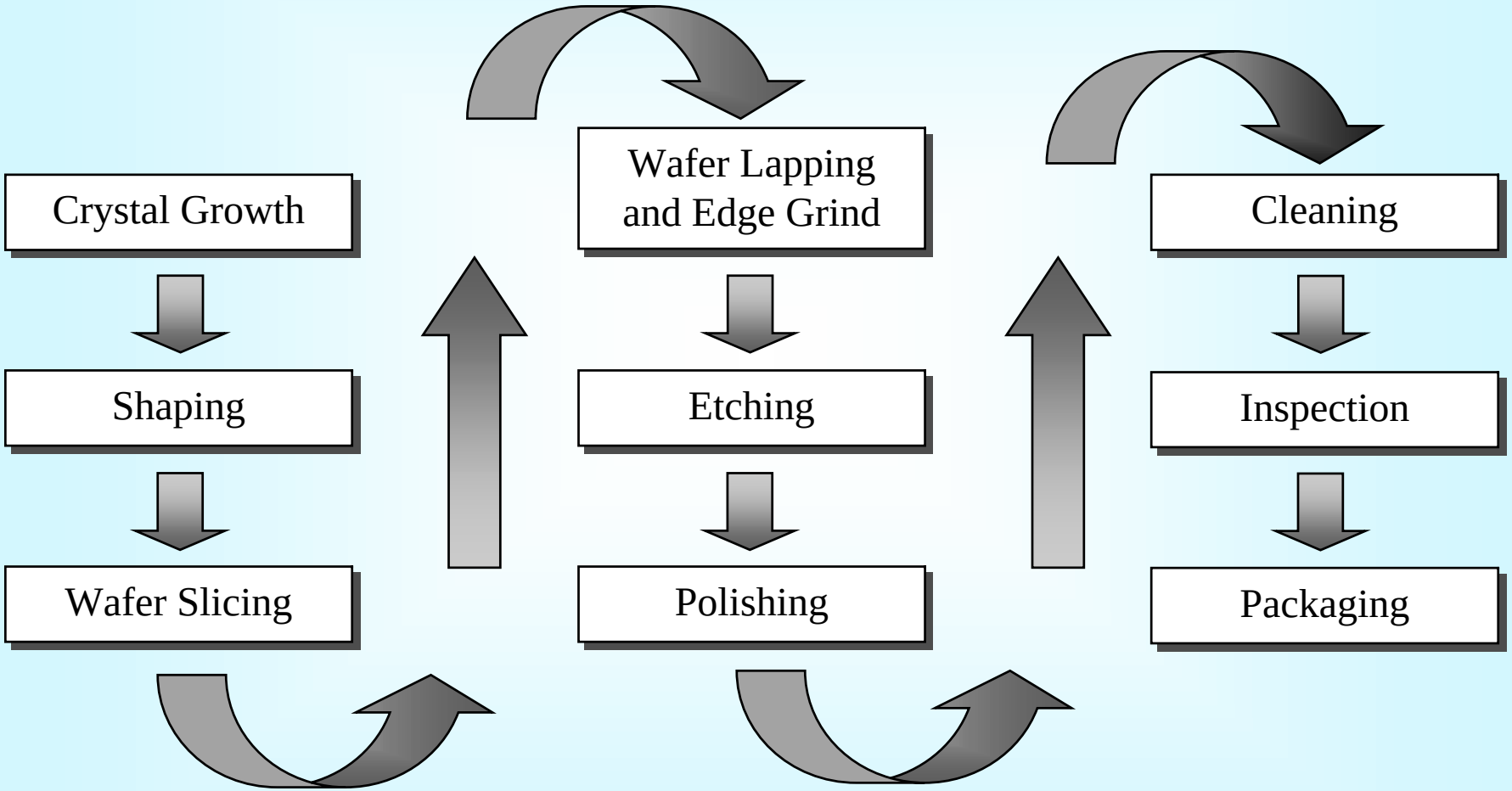
Common Dopants: Phosphorus, Boron, Arsenic

		Concentration (Atoms/cm^3)			
Dopant	**Material Type**	**$< 10^{14}$** (Very Lightly Doped)	**10^{14} to 10^{16}** (Lightly Doped)	**10^{16} to 10^{19}** (Doped)	**$>10^{19}$** (Heavily Doped)
Pentavalent	**n**	**n^{--}**	**n^{-}**	**n**	**n^{+}**
Trivalent	**p**	**p^{--}**	**p^{-}**	**p**	**p^{+}**

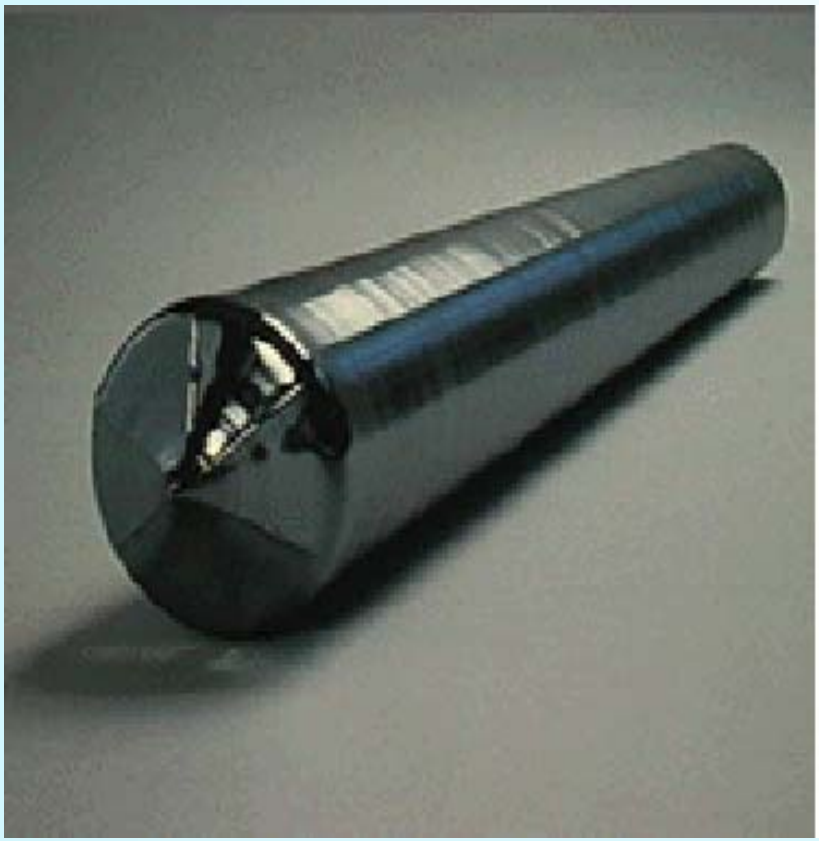
Segregation Fraction for FZ Refining

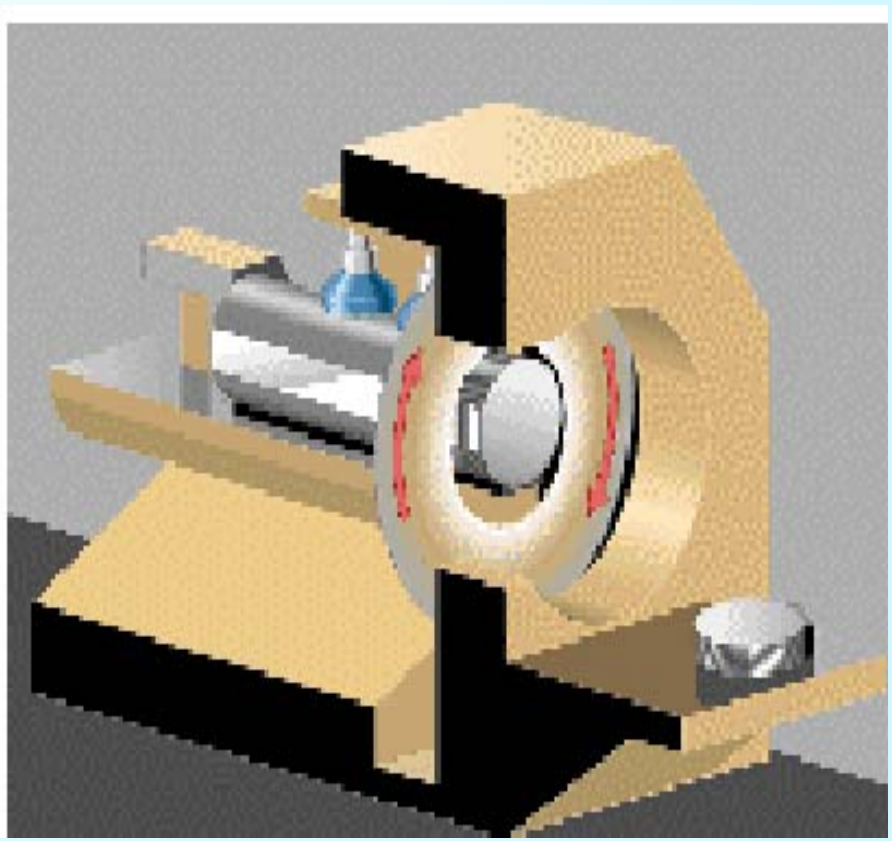


Basic Process Steps for Wafer Preparation

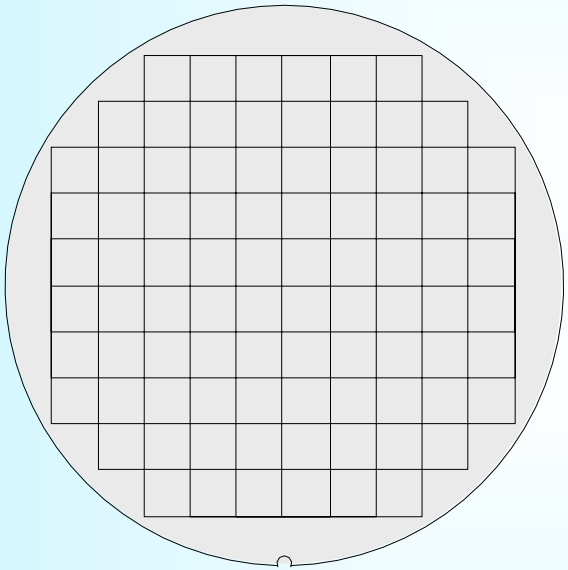


After crystal pulling, the boule is shaped and cut into wafers which are then polished on one side.



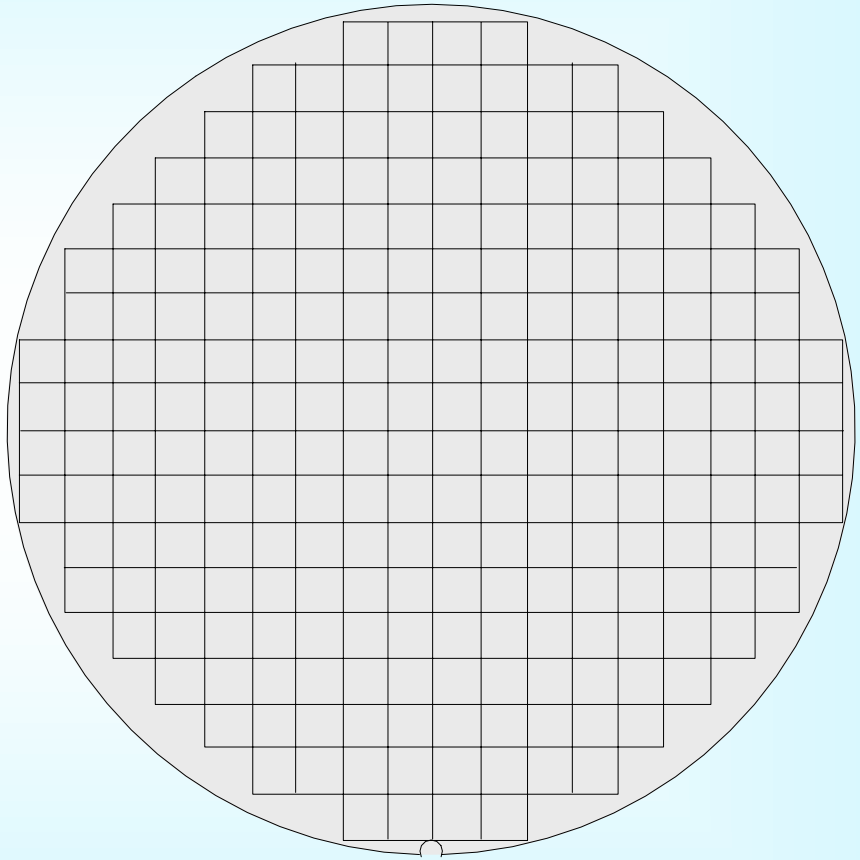


Increase in Number of Chips on Larger Wafer Diameters (Assume large 1.5 x 1.5 cm microprocessors)



88 die

200-mm wafer



232 die

300-mm wafer

Figure 4.13

Developmental Specifications for 300-mm Wafer Dimensions and Orientation

Parameter	Units	Nominal	Some Typical Tolerances
Diameter	mm	300.00	± 0.20
Thickness (center point)	μm	775	± 25
Warp (max)	μm	100	
Nine-Point Thickness Variation (max)	μm	10	
Notch Depth	mm	1.00	+ 0.25, -0.00
Notch Angle	Degree	90	+5, -1
Back Surface Finish		Bright Etched/Polished	
Edge Profile Surface Finish		Polished	
FQA (Fixed Quality Area – radius permitted on the wafer surface)	mm	147	

From H. Huff, R. Foodall, R. Nilson, and S. Griffiths, "Thermal Processing Issues for 300-mm Silicon Wafers: Challenges and Opportunities," ULSI Science and Technology (New Jersey: The Electrochemical Society, 1997), p. 139.

Table 4.4

Quality Measures

- Physical dimensions
- Flatness
- Microroughness
- Oxygen content
- Crystal defects
- Particles
- Bulk resistivity

Electron Microscopy (TEM) of SiO_2 on Si